AMENDMENTS TO THE SPECIFICATION

Please amend the title as follows:

Stacked columnar 1T-nMTJ [MRAM] structure and its method of formation and operation

In the "Related U.S. Application Data" section, please modify the following paragraph:

This is a division of Application No./10/214,167, filed August 8, 2002, and issued as U.S. Pat. No. 6,882,553 on April 19, 2005, the entire disclosure of which is incorporated herein by reference.

In the specification, please amend the following paragraphs:

[0001] The present invention relates to ~~magnetoresistive~~ random access memory ~~(MRAM)~~ devices and, more particularly, to read circuitry for such devices.

[0006] This invention provides an [MRAM] array read architecture which incorporates certain advantages from both cross-point and 1T-1MTJ architectures. The fast read-time and high signal to noise ratio of the 1T-1MTJ architecture and the higher packing density of the cross-point architecture are both exploited in the invention by uniquely combining certain characteristics of each. An access transistor is used to select for reading multiple columns of [MRAM] memory cells, which are stacked vertically

above one another in a memory slice of a memory array. In this architecture, the plurality of columns of [MRAM] memory cells share a common sense line. A specific [MRAM] memory cell within the multiple columns is accessed by a row and plane address during a read operation.

[0007] The invention also provides a method of fabricating ~~an MRAM~~ a memory device having the characteristics noted in the preceding paragraph and a method of operating the memory device to read a selected memory cell. These and other features and advantages will become more apparent from the following detailed description of the invention which is provided in conjunction with the accompanying drawings.

[0017] The terms "substrate" and "wafer" can be used interchangeably in the following description and may include any semiconductor-based structure. The structure should be understood to include silicon, silicon-on insulator (SOI), silicon-on-sapphire (SOS), doped and undoped semiconductors, epitaxial layers of silicon [Aupported] supported by a base semiconductor foundation, and other semiconductor structures. The semiconductor need not be silicon-based. The semiconductor could be silicon-germanium, germanium, or gallium arsenide. When reference is made to the substrate in the following description, previous process steps may have been utilized to form regions or junctions in or over the base semiconductor or foundation.

[0018] The fast read-time and high signal to noise ratio of the 1T-1MTJ architecture and the higher packing density of the cross-point architecture are both exploited by combining certain characteristics of each layout in the invention. As shown in FIGS. 1 and 2a . . . 2d, the array architecture of the invention has a plurality of memory arrays 34 stacked one over another. Each array 34 includes a plurality of rows and columns of memory cells. [AR] All of the memory cells in the corresponding

column in each of the stacked arrays form a memory slice 80 and are coupled to a single access transistor 16 as a group.

[0041] The primary bus bridge 903 is coupled to at least one peripheral bus 910. Various devices, such as peripherals or additional bus bridges may be coupled to the peripheral bus 910. These devices may include a storage controller 911, a miscellaneous I/O device 914, a secondary bus bridge 915, a multimedia processor 918, and a legacy device interface 920. The primary bus bridge 903 may also be coupled to one or more special purpose high speed ports 922. In a personal computer, for example, the special purpose port might be the Accelerated Graphics Port (AGP), used to couple a high performance video card to the processing system 900.

[0042] The storage controller 911 couples one or more storage devices 913, via a storage bus 912, to the peripheral bus 910. For example, the storage controller 911 may be a SCSI controller and storage devices 913 may be SCSI discs. The I/O device 914 may be any sort of peripheral. For example, the I/O device 914 may be a local area network interface, such as an Ethernet card. The secondary bus bridge may be used to interface additional devices via another bus to the processing system. For example, the secondary bus bridge may be [an] a universal serial port (USB) controller used to couple USB devices 917 via to the processing system 900. The multimedia processor 918 may be a sound card, a video capture card, or any other type of media interface, which may also be coupled to one of such additional devices such as speakers 919. The legacy device interface 920 is used to couple legacy devices, for example, older styled keyboards and mice, to the processing system 900.

[0043] The processing system 900 illustrated in FIG. 5 is only an exemplary processing system with which the invention may be used. While FIG. 1 illustrates a processing architecture especially suitable for a general purpose computer, such as a

personal computer or a workstation, it should be recognized that well known modifications can be made to configure the processing system 900 to become more suitable for use in a variety of applications. For example, many electronic devices, which require processing may be implemented using a simpler architecture, which relies on a CPU 901, coupled to memory components 908 and/or memory devices 100. These electronic devices may include, but are not limited to audio/video processors and recorders, gaming consoles, digital television sets, wired or wireless telephones, navigation devices (including ~~system~~ systems based on the global positioning system (GPS) and/or inertial navigation), and digital cameras and/or recorders. The modifications may include, for example, elimination of unnecessary components, addition of specialized devices or circuits, and/or integration of a plurality of devices.